Notice of Allowability	Application No.	Applicant(s)	
	10/531,756	RAUBUCH, MARTIN	
	Examiner	Art Unit	
	William B. Partridge	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed 9/22/2009*.

2. ☒ The allowed claim(s) is/are *1-10 and 14-28*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. ____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 9/22/2009
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other ____.

/William B Partridge/
Examiner, Art Unit 2183

EXAMINER'S AMENDMENT

1. The IDS filed 9/22/2009 has not been considered as copies of foreign patent documents and NPL have not been supplied as required.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with David Dolezal on 6/12/2009.

The application has been amended as follows (note, claims not mentioned remain as they were presented in the claims submitted on 01/21/2008):

1. (Currently Amended) An arrangement for vector permutation in a single- instruction multiple-data microprocessor, the arrangement comprising:

a vector register file;

a permutation logic block coupled to receive and permutate vectors from at least one vector register of the vector register file according to control parameters, the permutation of the vectors being [[as]] a side operation of an instruction;

a plurality of control registers separate from the vector register file, each of the plurality of control registers being coupled to selectively provide control parameters to the permutation logic block; and

a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting by an order one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

2. (Currently Amended) A single-instruction multiple-data microprocessor vector permutation system comprising:

at least one vector register;

a vector register file;

a permutation logic block coupled to receive and permutate vectors from the at least one vector register of the vector register file according to control parameters, the permutation of the vectors being [[as]] a side operation of an instruction;

a plurality of control registers separate from the vector register file, each of the plurality of control registers being coupled to selectively provide control parameters to the permutation logic block; and

a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting by an order one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

4. (Currently Amended) The arrangement of claim 1 wherein the controller control means includes at least one counter arranged to provide the order as a sequential order for selecting one of the plurality of control registers.

5. (Currently Amended) A method for vector permutation in a single-instruction multiple-data microprocessor, the method comprising the steps of:

providing vectors to be permutated in a vector register file; providing a plurality of control registers separate from the vector register file;

providing a controller coupled between the plurality of control registers and the permutation logic block;

selecting by an order one of a plurality of control registers, each control register containing parameters for determining permutation characteristics; and

permutating the vectors as a side operation of an instruction according to the parameters of the selected control register.

7. (Currently Amended) The method of claim 5 wherein the step of selecting by an order further includes the following of a sequential order of the plurality of control registers.

15. (Currently Amended) The system of claim 2 wherein the controller means includes at least one counter arranged to provide the order as a sequential order for selecting one of the plurality of control registers.

28. (Currently Amended) An arrangement for vector permutation in a single-instruction multiple-data microprocessor, the arrangement comprising:

a vector register file;

a permutation logic block coupled to receive and permutate vectors from at least one vector register of the vector register file according to control parameters, the permutation of the vectors being a side operation of an instruction;

a plurality of control registers separate from the vector register file, each of the plurality of control registers being coupled to selectively provide control parameters to the permutation logic block; and

a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting by an order one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block wherein the controller includes at least one counter arranged to provide the order as a sequential order for cyclically sequencing through the plurality of control registers.

29. (Canceled)

3. The following is an examiner's statement of reasons for allowance: the prior art of record fails to disclose the use of a vector permutation operation being performed as a side operation of another instruction wherein the vector register file and control registers are in separate register files and wherein there is a controller that selects the control registers in an order to control the vector permutation. While there is prior art of record to suggest vector permutations and the

notion of side operations, nothing in particular points to these being done together, much less in the way claimed, specifically with the selection mechanism being in order (e.g. a sequential order as per dependent claims). One of ordinary skill in the art would not have reason or motivation to combine any prior art of record to obtain the invention as disclosed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William B. Partridge whose telephone number is (571) 270-1402. The examiner can normally be reached on Mon-Fri 2PM - 6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William B Partridge/
Examiner, Art Unit 2183

/David J. Huisman/
Primary Examiner, Art Unit 2183